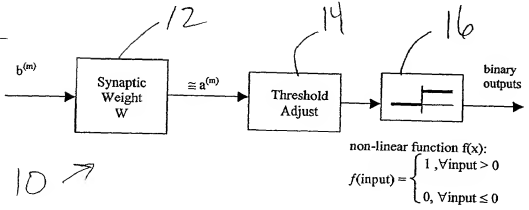
12
14
16
$b^{(m)}$
Synaptic Weight W
$\cong a^{(m)}$
Threshold Adjust
binary outputs
10
non-linear function f(x):
$f(\text{input}) = \begin{cases} 1, \forall \text{input} > 0 \\ 0, \forall \text{input} \leq 0 \end{cases}$

Fig. 1

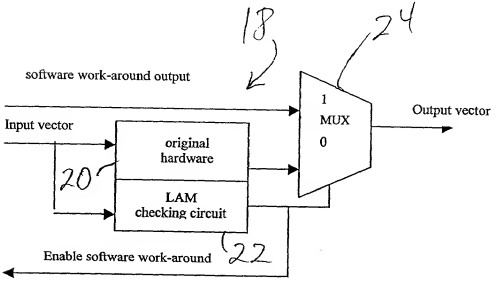
18
24
software work-around output
Input vector
original hardware
20
LAM checking circuit
1
MUX
0
Output vector
Enable software work-around
22

Fig. 2

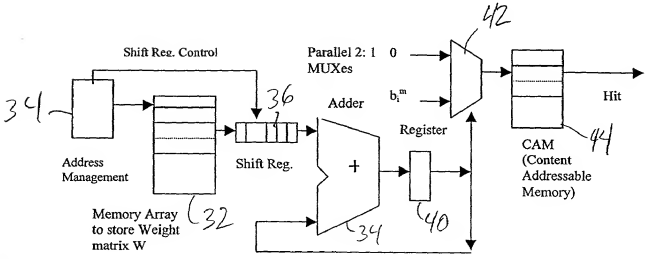
Shift Reg. Control
Parallel 2: 1 MUXes
0
42
34
36
Adder
b_i^m
Hit
Register
Address Management
Shift Reg.
+
CAM (Content Addressable Memory)
44
Memory Array to store Weight matrix W
32
34
40
30

Fig. 3

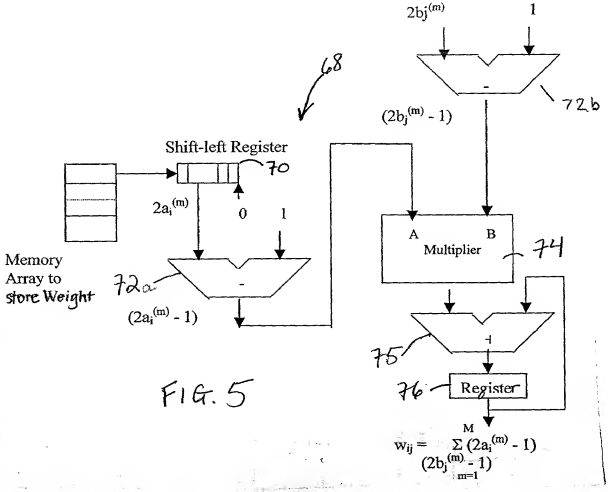
68
$2b_j^{(m)}$
1
-
72b
$(2b_j^{(m)} - 1)$
Shift-left Register
70
$2a_i^{(m)}$
0
1
A
B
Multiplier
74
Memory Array to store Weight
72a
$(2a_i^{(m)} - 1)$
+
75
76
Register
$w_{ij} = \sum_{m=1}^{M} (2a_i^{(m)} - 1)(2b_j^{(m)} - 1)$

FIG. 5

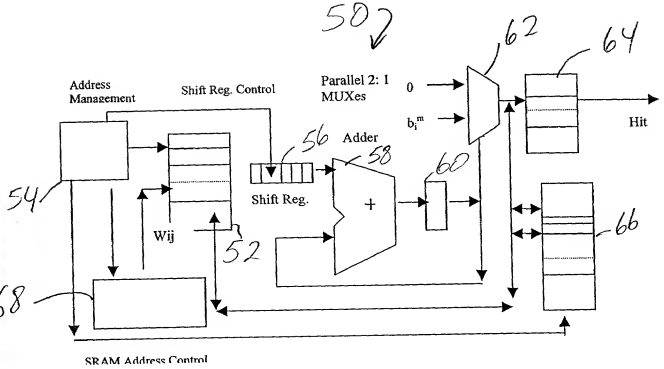
50
62
64
Address Management
Shift Reg. Control
Parallel 2: 1 MUXes
0
b_i^m
Hit
56
Adder
58
60
54
Shift Reg.
+
Wij
52
66
68
SRAM Address Control

Fig. 4